

Hunter Blake Estes

Graduate Student, NSF-IGERT Fellow

<http://research.engr.utexas.edu/igertsustainablegrids/>

Focus: Energy & Power Systems

Research Advisors:

Dr. Alexis Kwasinski & Dr. Robert Hebner

Research Group: Center for Electromechanics

<http://www.utexas.edu/research/cem/dcmicrogridfaultexperiments.html>

- **The University of Texas at Austin**
Department of Electrical & Computer Engineering
graduate work (24 hrs)
undergraduate work (46 hrs) – *no degree sought*
- **7+ years Semiconductor Industry**
Diffusion Process & Integration engineer
(AMD, Honeywell, STMicroelectronics)
- **The University of Texas at Austin**
Department of Chemical Engineering (BS – Dec.'97)

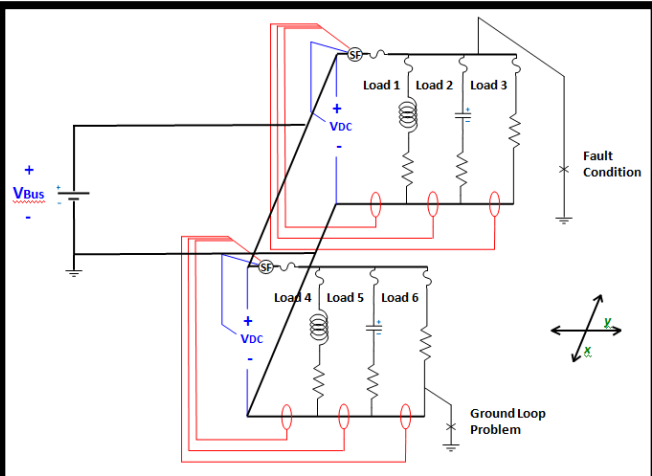
PUBLICATIONS

- **Masters Thesis (in review):** “*Open Series Fault Comparison in AC & DC Micro-grid Architectures*”, The University of Texas, Dept. of Electrical & Computer Engineering – Dr. Kwasinski & Dr. Hebner
- **Conf. Paper:** “*Open Series Fault Comparison in AC & DC Micro-grid Architectures*”, **primary author**, The International Telecommunications Energy Conference (INTELEC) 2011 – Amsterdam, The Netherlands
- **Conf. Paper:** “*Development of a Series Fault Model for DC Micro-grids*”, **co-author**, PES Innovative Smart Grid Technologies Conference 2012 – Washington, D.C., USA
- **Conf. Presentation:** “*DC Open Series Fault Considerations for Distributed Generation μ Grid Architecture*”, **sole presenter**, Electric Ship Technologies Symposium (ESTS) 2011 – Alexandria, VA, USA

RESEARCH AWARDS, GRANTS, & FUNDING

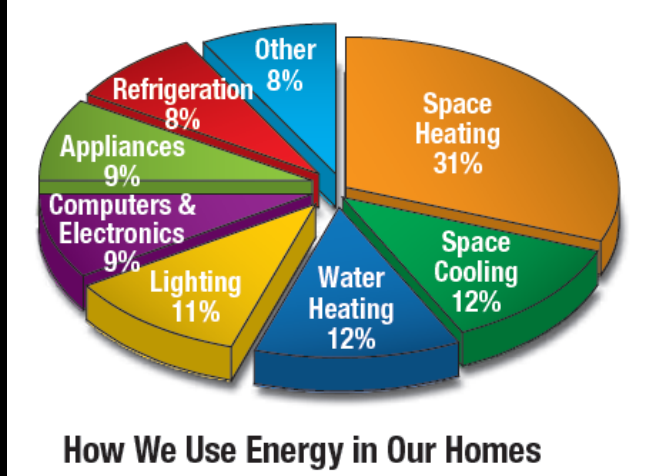
- National Science Foundation (NSF) – IGERT Graduate Fellow / Trainee – *Fall '10 – Spring '12*
(<http://research.engr.utexas.edu/igertsustainablegrids/>)
 - Internship – Technische Universität München – Munich, Germany – *Summer '11*
 - Graduate Researcher – Pecan Street, Inc. – Austin, TX (<http://www.pecanstreet.org/>)
- Al F. Tasch, Jr. Memorial Endowed Graduate Fellowship – UT Austin, Dept. of ECE, – *Fall '10-Spring '11*
- Graduate Research Assistant – Dr. Hebner – UT Austin, Center for Electromechanics – *Fall '10 - current*

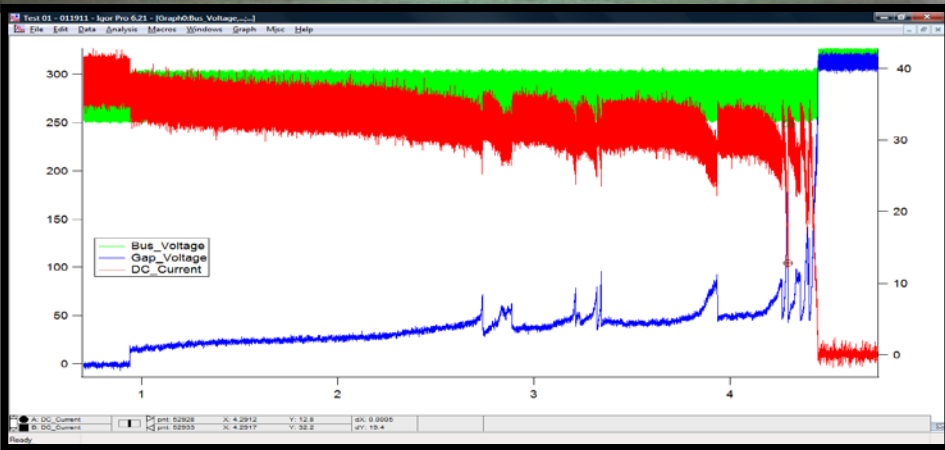
- With the recent interest in **smart grid** technology, **active power management**, **distributed generation**, **energy storage**, etc., DC architectures are gaining more attention. Especially if power is generated locally, or does not have to travel far from source to load. (*old Tesla & Westinghouse vs. Edison debate, revisited?*)
- Many Distributed Generation **resources** generate in DC:
 - solar PV arrays, fuel cells, microturbines, **batteries**, ultracapacitors, rectified wind systems*
- Many **loads** are, or can be DC-based:
 - LEDs, computers & electronics, appliances, electric heating, AC compressor induction motors can be replaced by DC brush(less) motors, **EVs**, etc.*
- Advanced Power Electronics** now allow for DC-DC conversions, as well as some branch isolation techniques (*something not available 100 years ago*)
- However, with the lack of a periodic zero-crossing, the biggest concern with DC systems is what happens during a **fault** condition. (*i.e. **safety considerations***)
- Research topic is therefore on DC micro-grids with a particular emphasis on **open series fault formations & their effects** on localized grid



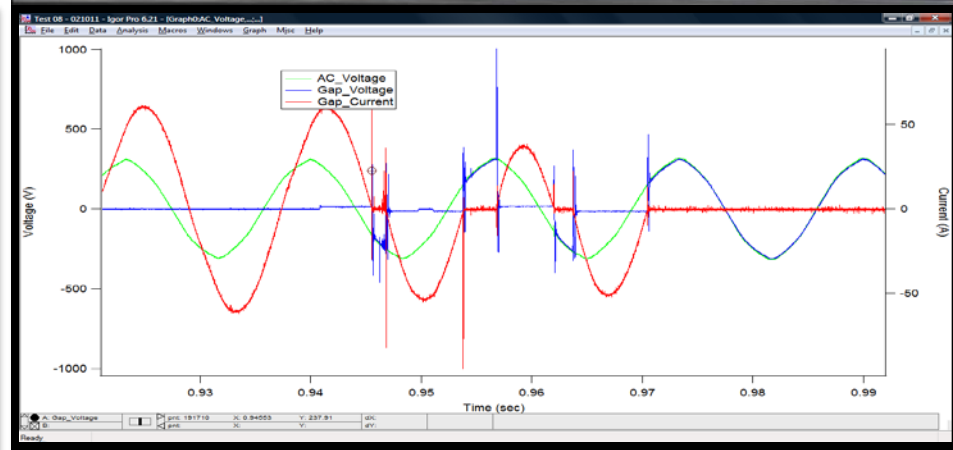
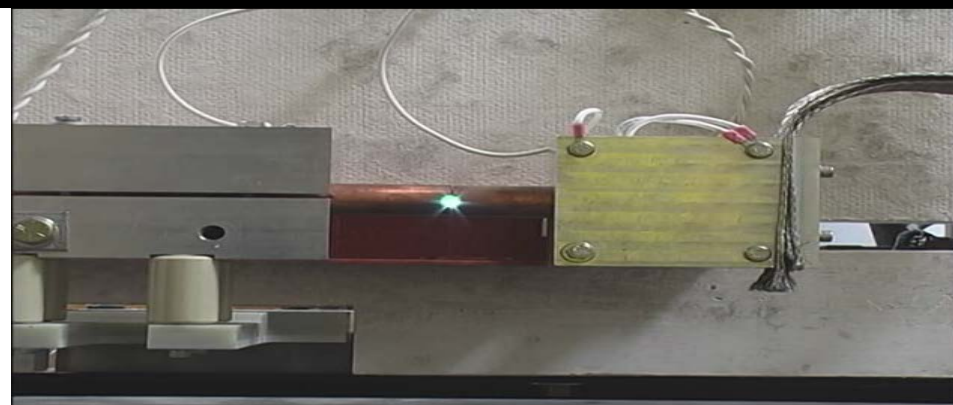
Hunter Blake Estes
Graduate Research
Topic

UNIVERSITY OF TEXAS AT AUSTIN
UT ECE
 ELECTRICAL & COMPUTER ENGINEERING





DC open series fault transients



AC open series fault transients

- **Experimental approach** by 1st building a μ Grid:
 - 3 ϕ AC source panel \rightarrow variac or transformer \rightarrow passive 6 diode bridge rectifier (DBR) \rightarrow “open series fault” \rightarrow R-L load
 - DC (280 – 635V) vs. AC systems of “quasi-equivalent” parameters
- **Monitor:** currents, gap voltages, arc fault transients, power dissipated, bus disturbances, duration, re-strikes, & impedance effects (50 to 5 μ s data capture rates, 12 bit resolution)
- **Model:** DC arc transient effects, grid propagation of these disturbances, etc.
- **Suggest:** DC breaker designs, DC architecture fault clearing strategies, safety recommendations
- **Further Study:** DC positive voltage single line-to-ground faults, ground loop faults, etc.